



<b>INFORMATION DISCLOSURE CITATION</b> PTO-1449		Customer Number <b>26615</b>	ATTORNEY'S DKT No. H1492	APPLICATION No. 10/653,105			
			APPLICANT(S) Bin Yu et al.				
			FILING DATE September 3, 2003	GROUP <del>2829</del> 2811			
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
<u>Vu</u>	US 2002/0125536 A1	09-12-02	Iwasa et al.	257	368	07-18-01	
<u>Vu</u>	US 2002/0153587 A1	10-24-02	Adkisson et al.	257	510	07-02-02	
<u>Vu</u>	US 2002/0177263 A1	11-28-02	Hanafi et al.	438	183	05-24-01	
<u>Vu</u>	6,359,311 B1	03-19-02	Colinge et al.	257	347	01-17-01	
<b>FOREIGN PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
<u>Vu</u>	Jong-Tae Park et al.: "Multiple-Gate SOI MOSFETs: Device Design Guidelines," <i>IEEE Transactions on Electron Devices</i> , Vol. 49, No. 12, December 2002, pp. 2222-2229.						
	Fu-Liang Yang et al.: "25 nm CMOS Omega FETs," International Electron Devices Meeting 2002, IEDM, Technical Digest, December 8-11, 2002 in New York, NY, pp. 255-258.						
	Toshikazu Mukaiyama et al.: "Fabrication of Gate-All-Around MOSFET By Silicon Anisotropic Etching Technique," <i>Solid State Electronics</i> , Elsevier Science Publishers, Vol. 42, No. 7-8, July 8, 1998, pp. 1623-1626.						
	Yang-Kyu Choi et al.: "Spacer FinFET: nanoscale double-gate CMOS technology for the terabit era," <i>Solid State Electronics</i> , Elsevier Science Publishers, Vol. 46, No. 10, October 2002, pp. 1595-1601.						
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<u>Vu</u>	PCT International Search Report mailed July 13, 2004, 5 pages.						
EXAMINER <b>HUNG VU</b>			DATE CONSIDERED <b>8/02/04</b>				

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).